SONY

CXG1010N

Power Amplifier for PHS

Description

The CXG1010N is a power amplifier for PHS. This IC is designed using the Sony's GaAs J-FET process and operates at a single power supply.

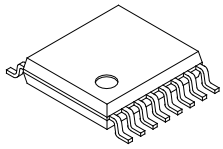
Features

- High output power 21.5 dBm
- Positive power supply drive V_{DD}=3.4 V
- Low current consumption 200 mA
- High gain 40 dB Typ.
- Low distortion (ACP) –59 dBc Typ.
- Small mold package 16-pin SSOP

Structure

GaAs J-FET MMIC

16 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{DD}	6	V
• Voltage between gate and source	Vgs0	1.5	V
• Drain current	I_{DD}	500	mA
• Power dissipation	P_D	3	W
• Channel temperature	Tch	175	°C
• Operating temperature	Top	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

Electrical Characteristics

V_{DD}=3.4 V, V_{CTL}=2.0 V, f=1.90 GHz (Ta=25 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
*1 Current consumption	I_{DD}		200		mA
*1 Gate voltage adjustment value	V_{GG2}	0	0.5	1.0	V
Input VSWR	$VSWR_{IN}$		1.5	2.0	—
Output power (for –15.5 dBm input)	P_{OUT}	21.5			dBm
*2 Power gain	G_P	37	40	43	dB
*2 *3 Gain control	G_{CTL}		20		dB
*2 Average leak power level (600 kHz±100 kHz)	$P_{LEAK600}$		–59	–54	dBc
*2 Average leak power level (900 kHz±100 kHz)	$P_{LEAK900}$		–65	–59	dBc

*1 This value is adjusted by V_{GG1} and V_{GG2} set with Sony's recommended current adjustment method when 21.5 dBm is output. In this time, the voltage ratio of V_{GG1} and V_{GG2} should match to the voltage ratio generated by the resistance of the recommended gate bias circuit.

*2 When 21.5 dBm is output.

*3 $G_{CTL}=G_P$ (V_{CTL} 2.0 V)–G_P (V_{CTL} 0 V)

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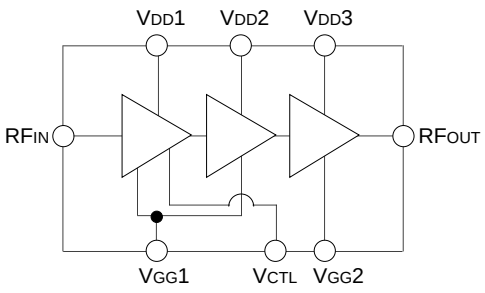
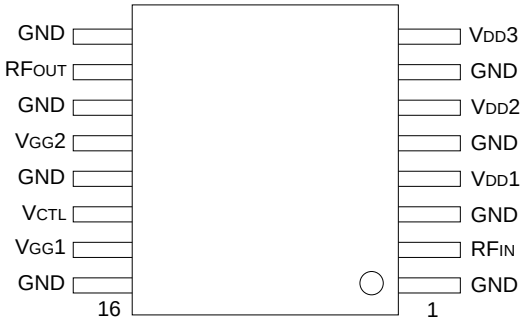
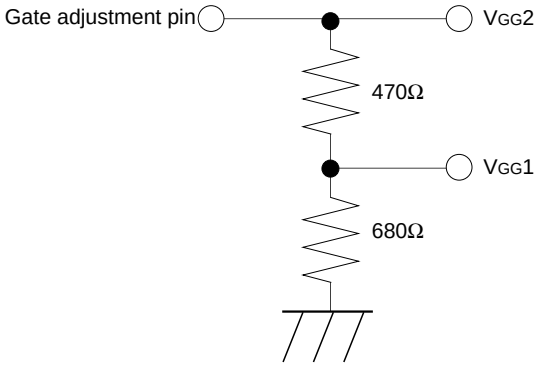
Block Diagram



Pin Configuration



Gate adjustment pin



Recommended Current Adjustment Method

(1) $V_{GG}2$/PIN separate adjustment

($V_{GG}2$ adjustment 1)	(PIN adjustment 1)	($V_{GG}2$ adjustment 2)	(PIN adjustment 2)
When the RF input (PIN) is off, the current consumption (I_{DD}) is adjusted to 200 mA.	The output power (P_{OUT}) is adjusted to 21.5 dBm.	The current consumption (I_{DD}) is finely adjusted to 200 mA.	The output power (P_{OUT}) is finely adjusted to 21.5 dBm.
Variation of I_{DD} and P_{OUT} due to adjustment	I_{DD}=200±20 mA P_{OUT}=21.5 dBm	I_{DD}=200 mA P_{OUT}=21.5±0.2 dBm	I_{DD}=200±5 mA P_{OUT}=21.5 dBm

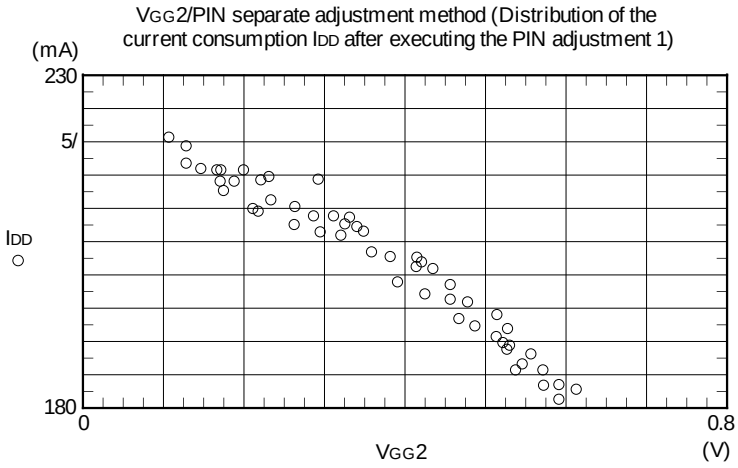
(2) Simple adjustment

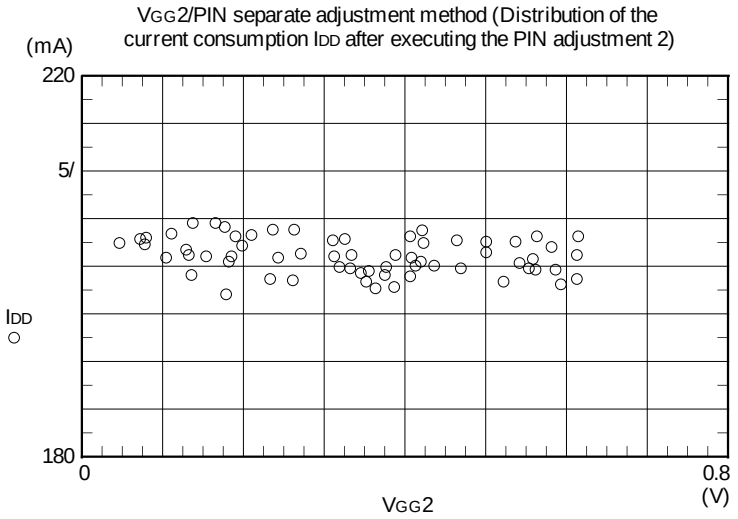
(I_{DD} read)	($V_{GG}2$ setting)	(PIN adjustment)
When the RF input (PIN) is off, the gate voltage ($V_{GG}2$) is set to 0.4 V and it is read.	The formula*1 where $V_{GG}2=f(I_{DD}: V_{GG}2=0.4\ V)$ is used to set $V_{GG}2$.	The output power (P_{OUT}) is adjusted to 21.5 dBm.
Variation of I_{DD} and P_{OUT} due to adjustment	*1 e.g. $V_{GG}2=a-b \times I_{DD}$	I_{DD}=200±5 mA P_{OUT}=21.5 dBm

Current Consumption Variation with Recommended Current Adjustment Method

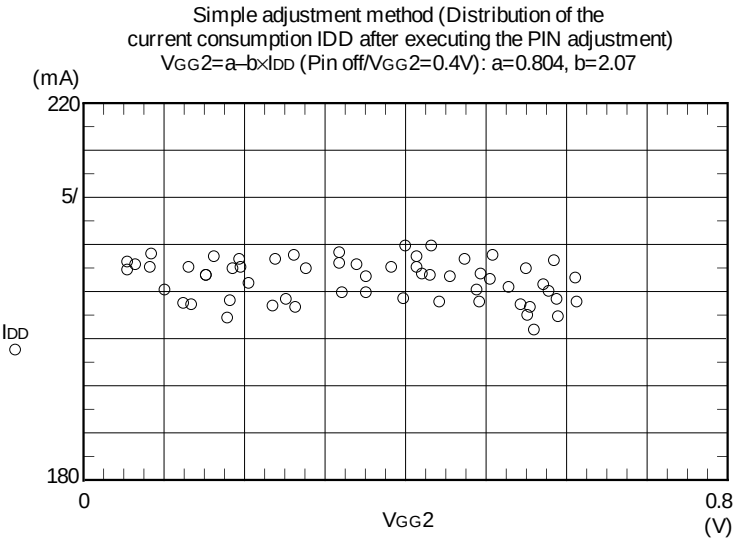
(For P_{OUT}=21.5 dBm output)

(1) Separate adjustment

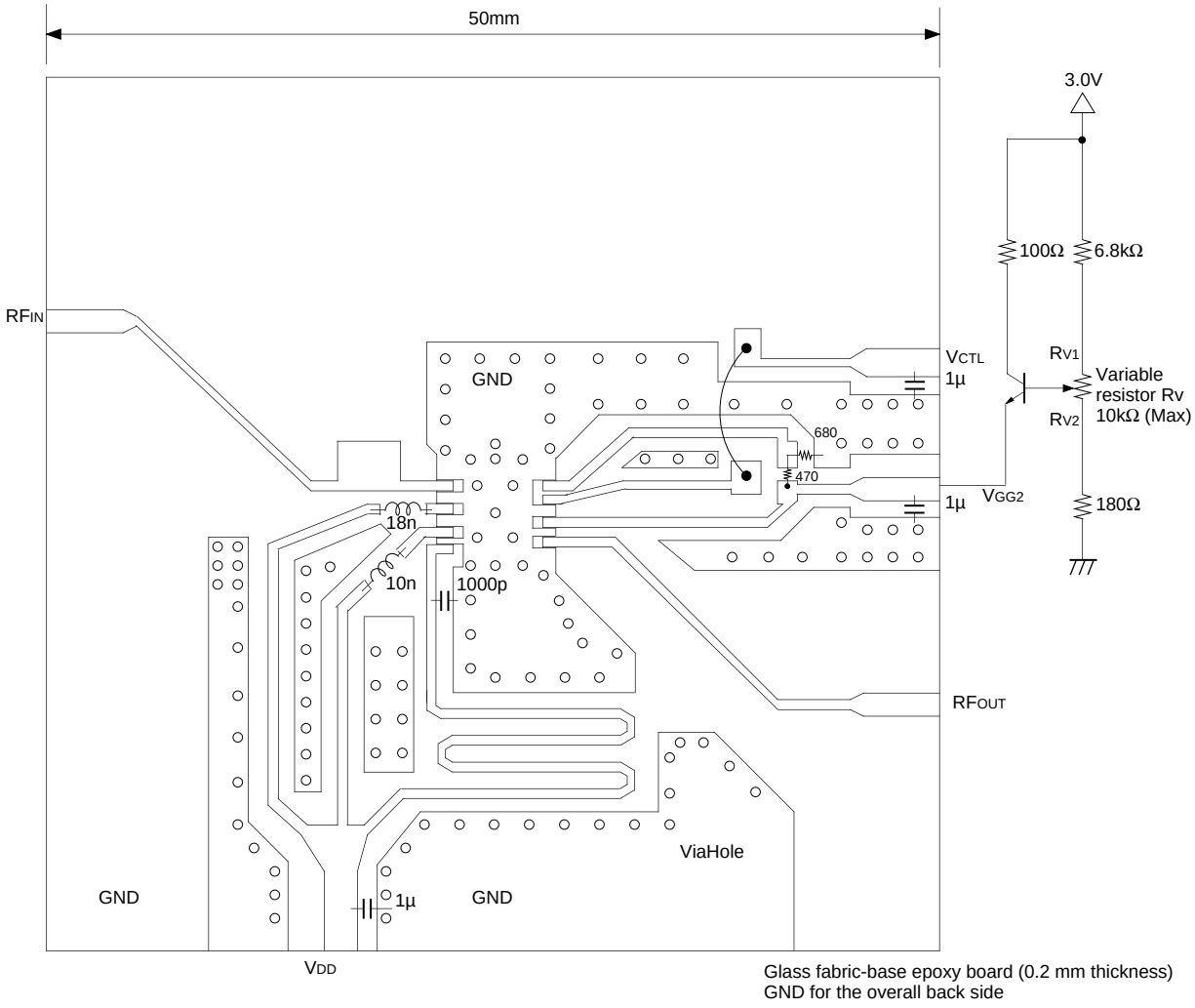




(2) Simple adjustment

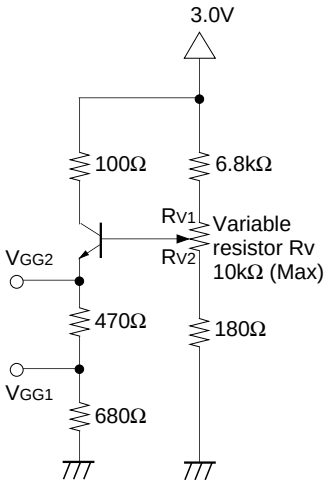


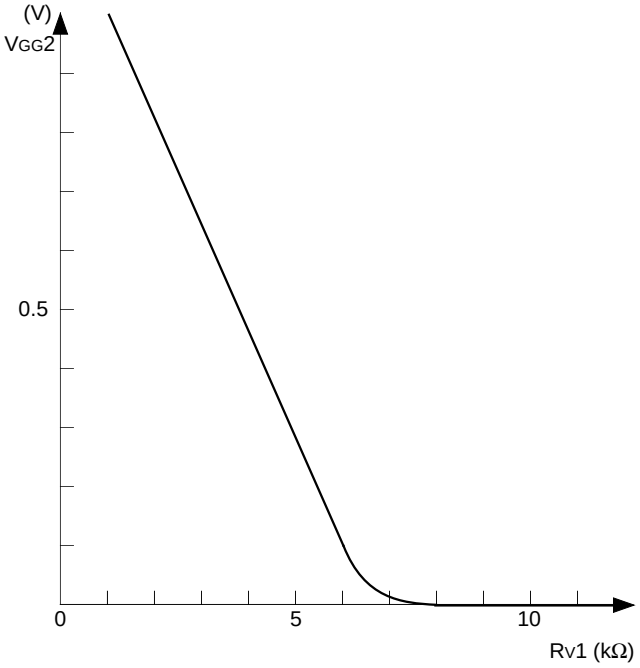
Recommended Evaluation Circuit



Glass fabric-base epoxy board (0.2 mm thickness)
GND for the overall back side

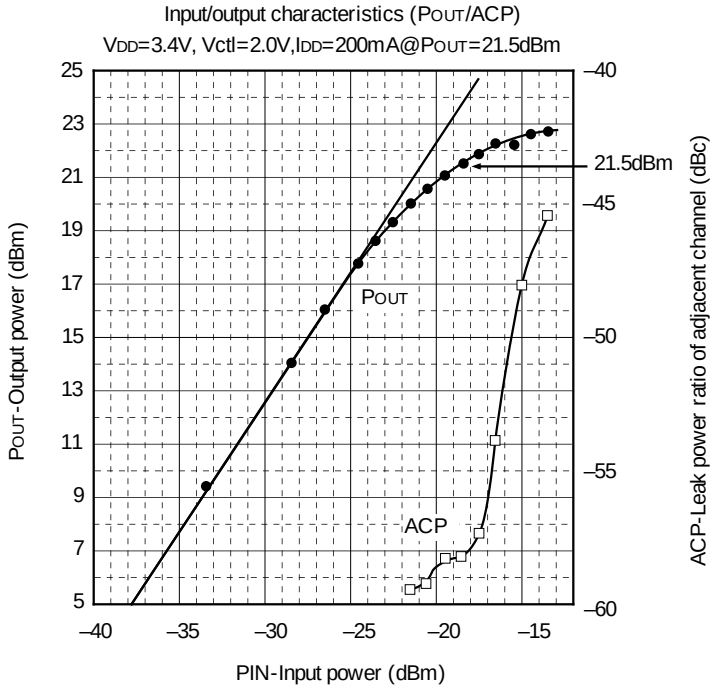
Recommended Gate Bias Circuit and Circuit Characteristics

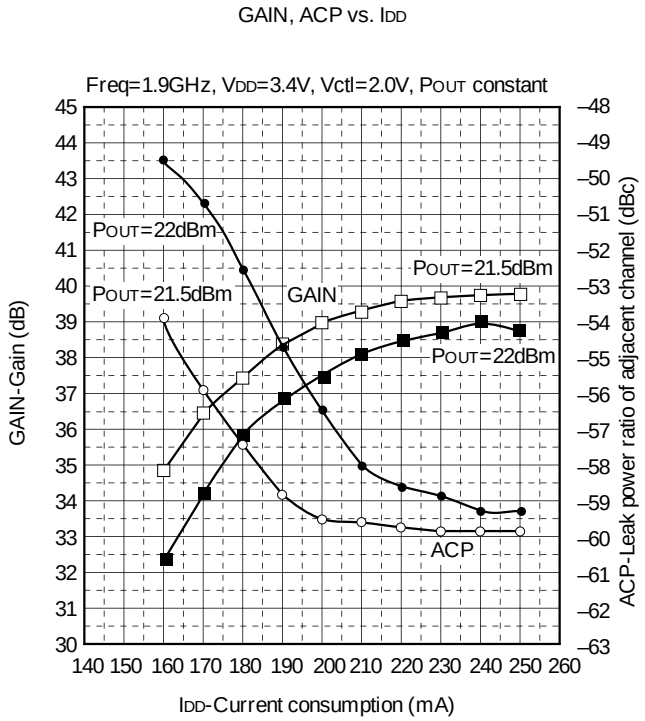


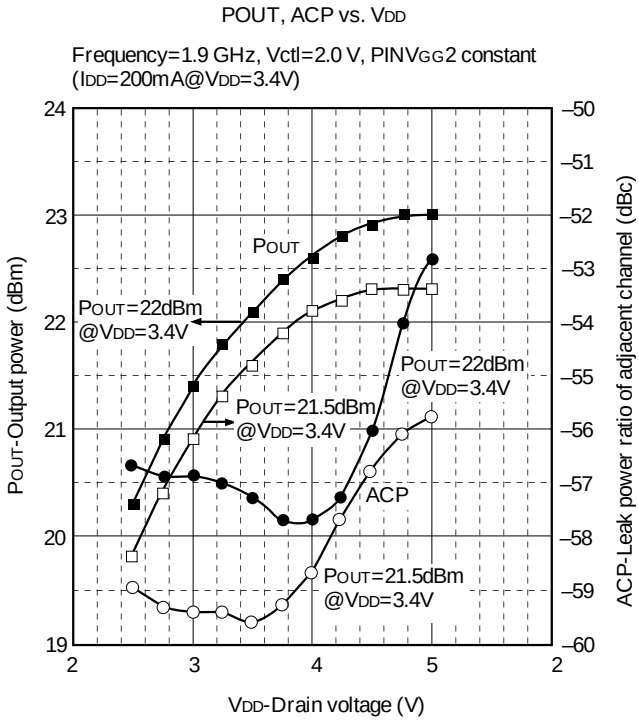


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Example of Representative Characteristics (Ta=25 °C)

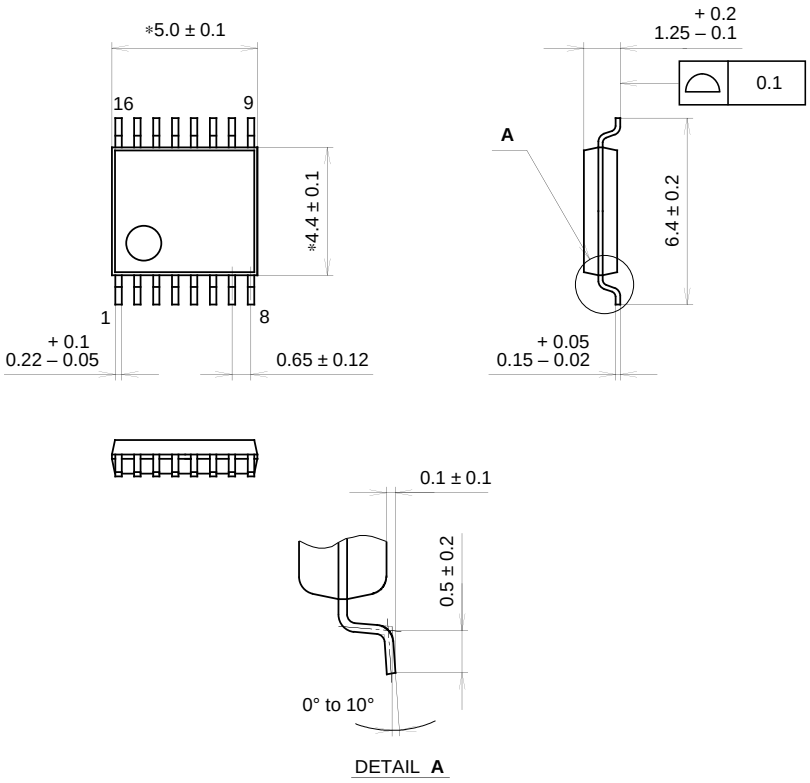






Package Outline Unit : mm

16PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-16P-L01
EIAJ CODE	SSOP016-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.1g